Amendments to the Claims

The following listing of the claims will replace all prior versions, and listings of the claims in the application:

Listing of Claims

1-16 Canceled

17. (Previously presented) A method for self-routing a packet to a given destination address through a bit-permuting network having 2^n input ports and 2^n output ports, the network being characterized by a guide, the method comprising:

generating a routing tag for the packet based on the guide of the network and the destination address, and

routing the packet through the network using the routing tag.

18. (Previously presented) The method as recited in claim 17, wherein the network is a k-stage network composed of nodes and the destination address is expressed as binary($d_1 d_2 \ldots d_k$) and the guide is expressed as $\gamma(1), \gamma(2), \ldots, \gamma(k)$ where γ is a mapping from the set $\{1, 2, \ldots, k\}$ to the set $\{1, 2, \ldots, n\}$, and wherein the generating of the routing tag includes generating binary ($d_{\gamma(1)} d_{\gamma(2)} \ldots d_{\gamma(k)}$).

19. (Previously presented) The method as recited in claim 18, including prepending the binary ($d_{\gamma(1)} d_{\gamma(2)} \ldots d_{\gamma(k)}$) to the packet.

20. (Previously presented) The method as recited in claim 19, wherein, for a j-th stage node, the routing includes using $d_{\gamma(j)}$ in the j-th stage node to select an output from the j-th stage node to emit the packet, $1 \leq j \leq k$.

21. (Previously presented) The method as recited in claim 20, wherein the network is an

n-stage banyan-type network, the guide ~~is~~ being expressed as $\gamma(1), \gamma(2), \ldots, \gamma(n)$ where γ is a permutation on the integers from 1 to n and wherein, for a j-th stage node, the routing includes using $d_{\gamma(j)}$ in the j-th stage node to select an output from the j-th stage node to emit the packet, $1 \leq j \leq n$.

22. (Previously presented) A method for self-routing a packet through a $2^n x 2^n$ switch, the switch having 2^n external output ports labeled with 2^n distinct binary output addresses in the form of $b_1 b_2 \ldots b_n$, and comprising a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by a guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$, where γ is a mapping from the set $\{1, 2, \ldots, k\}$ to the set $\{1, 2, \ldots, n\}$, wherein each of the switching cells is a sorting cell associated with the partial order "0 ('0-bound') < 1 ('1-bound')", the packet being destined for a binary output address $d_1 d_2 \ldots d_n$, the method comprising:

generating a routing tag $d_{\gamma(1)} d_{\gamma(2)} \ldots d_{\gamma(k)}$ for the packet based on the guide and the destination output address of the packet, and

routing the packet through the network by using $d_{\gamma(j)}$ in the routing tag in the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-th stage cell to emit the packet.

23. (Previously presented) The method as recited in claim 22, wherein the routing includes removing the bit $d_{\gamma(j)}$ from the routing tag before the packet exits the j-th stage cell, $1 \leq j \leq k$.

24. (Previously presented) The method as recited in claim 22, wherein the routing includes using a leading bit in the routing tag in the j-th stage cell, $1 \leq j \leq k$, to select the output from the j-th stage cell to emit the packet.

25. (Previously presented) The method as recited in claim 22, wherein the routing includes removing a leading one bit from the routing tag of the packet before the packet exits the j-th stage cell, $1 \leq j \leq k$, such that the leading bit of the routing tag in the j-th stage cell, $1 \leq j \leq k$, is always $d_{\gamma(j)}$.

26. (Previously presented) The method as recited in claim 22, wherein the routing includes rotating a leading one bit of the routing tag of the packet to the end of the routing tag

before the packet exits the j-th stage cell, $1 \leq j \leq k$, such that the leading bit of the routing tag in the j-th stage cell, $1 \leq j \leq k$, is always $d_{\gamma(j)}$.

27. (Previously presented) The method as recited in claim 22, wherein the switch is characterized as an n-stage banyan-type network with guide $\gamma(1), \gamma(2), \ldots, \gamma(n)$, where γ is a permutation on the integers from 1 to n and wherein the generating a routing tag includes generating $d_{\gamma(1)}d_{\gamma(2)}\ldots d_{\gamma(n)}$.

28. Canceled

29. (Previously presented) The method as recited in claim 22, wherein the sorting cell is associated with the partial order "10 ('0-bound') < 00 ('idle') < 11 ('1-bound')".

30. (Previously presented) The method as recited in claim 22, wherein generating the routing tag includes generating the routing tag $1d_{\gamma(1)}d_{\gamma(2)}\ldots d_{\gamma(k)}$ for a real data packet.

31. (Previously presented) The method as recited in claim 30, wherein the routing includes using $1d_{\gamma(j)}$ in the routing tag of the real data packet in the j-th stage cell, $1 \leq j \leq k$, to select the output from the j-th stage cell to emit the real data packet.

32. (Previously presented) The method as recited in claim 31, wherein the routing includes removing the bit $d_{\gamma(j)}$ from the routing tag before the real data packet exits from the j-th stage cell, $1 \leq j \leq k$.

33. (Previously presented) The method as recited in claim 31, wherein the routing includes using the leading two bits in the routing tag in the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-th stage cell to emit the packet.

34. (Previously presented) The method as recited in claim 33, wherein the routing includes removing a second leading one bit of the two leading bits from the routing tag of the

packet before the packet exits the j-th stage cell, $1 \leq j \leq k$, such that the leading two bits of the routing tag in the j-th stage cell, $1 \leq j \leq k$, are always $1d_{\gamma(j)}$.

35. (Previously presented) The method as recited in claim 33, wherein the routing includes rotating the second bit of the routing tag of the packet to the end of the routing tag before the packet exits the j-th stage cell, $1 \leq j \leq k$, such that the leading two bits of the routing tag in the j-th stage cell, $1 \leq j \leq k$, are always $1d_{\gamma(j)}$.

36. (Previously presented) A method for self-routing a plurality of real data packets through a $2^n x 2^n$ switch, the switch having 2^n external output ports labeled with 2^n distinct binary output addresses in the form of $b_1b_2...b_n$, and is composed of a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by ~~the~~ a guide $\gamma(1)$, $\gamma(2), \ldots, \gamma(k)$ where γ is a mapping from the set $\{1, 2, \ldots, k\}$ to the set $\{1, 2, \ldots, n\}$, wherein each of the switching cells is a sorting cell associated with the partial order "10 ('0-bound') < 00 ('idle') < 11 ('1-bound')", each of the real data packets arriving at a distinct external input port determining an active input port and being destined for a binary destination address $d_1d_2...d_n$, the method comprising:

generating an idle packet as a stream of '0' bits at each of the non-active external input ports,

generating a routing tag $1d_{\gamma(1)}d_{\gamma(2)}...d_{\gamma(k)}$ for each of the real data packets based on the guide of the network and the destination address of the packet,

generating a routing tag which is a string of k+1 '0' bits for each of the idle packets, and

routing the real data packets and the idle packets through the network by sorting the packets by the sorting cells of the network, wherein the sorting by each of the sorting cells is according to the associated partial order and is based upon the leading two bits, which are either '10' or '11' for a real data packet, or '00' for an idle packet, of the routing tag of each of the two packets arrived at each of the cells, and wherein the second leading bit is removed from the routing tag or rotated to the end of the routing tag of each of the packets before the packet exits from the j-th stage cell such that the leading two bits of the routing tag of each of the packets at each of the j-th stage cell, $1 \leq j \leq k$, are always '$1d_{\gamma(j)}$' or '00'.

37. (Previously presented) The method as recited in claim 36, wherein the real data packets are classified into 2^r priority classes, $r \geq 1$, wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, and the generating of a routing tag for each of the real data packets includes generating $1d_{\gamma(1)}p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag.

38. (Previously presented) The method as recited in claim 36, wherein the generating of a routing tag for each of the idle packets includes generating a string of k+r+1 '0' bits as the routing tag.

39. (Previously presented) The method as recited in claim 36, wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, the generating of a routing tag for each of the real data packets includes generating $1d_{\gamma(i)}p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag, the sorting at each of the sorting cells of a concentrator based upon the two leading bits of the routing tag includes using the priority code $p_1 \ldots p_r$ as the tiebreaker, and processing the routing tag includes generating the routing tag such that the leading r+2 bits of the routing tag of each of the real data packets at each of the j-th super-stage concentrators, $1 \leq j \leq k$, is '$1d_{\gamma(j)}p_1 \ldots p_r$'.

40. (Previously presented) The method as recited in claim 36, wherein the real data packets are classified into 2^r priority classes, $r \geq 1$, wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, the generating of a routing tag for each of the real data packets includes generating $1d_{\gamma(1)}p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag, the generating of a routing tag for each of the idle packets includes generating a string of k+r+1 '0' bits as the routing tag, the sorting at each of the sorting cells of the concentrator based upon the two leading bits of the routing tag includes using the priority code $p_1 \ldots p_r$ as the tiebreaker, and processing the routing tag includes removing the second leading bit from the routing tag or rotating the second leading bit to the end of the routing tag, and rotating the r-bit priority code $p_1 \ldots p_r$ to the position behind the next bit originally following the priority code in the routing tag such that the leading r+2 bits of the routing tag of each of the packets at each of the j-th super-stage concentrators, $1 \leq j \leq k$, are always '$1d_{\gamma(j)}p_1 \ldots p_r$' or '00...0'.

41. (Previously presented) A $2^n x 2^n$ self-routing switch having an array of 2^n external input ports and an array of 2^n external output ports with 2^n distinct binary output addresses in the form of $b_1 b_2 \ldots b_n$ for switching a packet, the packet being either a real data packet destined for an n-bit binary destination address, or being an idle packet having no pre-determined destination output address, the switch comprising:

a switch fabric with external switch fabric input ports, the switch fabric having a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by a guide $\gamma(l), \gamma(2), \ldots, \gamma(k)$, where γ is a mapping from the set $\{1, 2, \ldots, k\}$ to the set $\{1, 2, \ldots, n\}$,

a routing tag circuit, coupled to the external switch fabric input ports, for generating a routing tag $1 d_{\gamma(1)} d_{\gamma(2)} \ldots d_{\gamma(k)}$ for each of the real data packets based on the guide of the bit-permuting network and the destination output address of the packet, and

a routing control circuit, coupled to the switching cells, for routing the real data packet through the switch by using $ld_{\gamma(j)}$ in the routing tag of the packet in the j-th stage cell, $l \leq j \leq k$, to select an output from the j-th stage cell to emit the packet.

42. (Previously presented) The system as recited in claim 41, wherein the real data packets are classified into 2^r priority classes, $r \leq l$, wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, and wherein the routing tag circuit includes a generator for generating a routing tag for each of the real data packets of the form $ld_{\gamma(1)} p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag.